IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Yasuo YAMAGISHI, et al.**

Serial Number: **Not Yet Assigned**

Filed: **July 18, 2003**

For: **PROBE CARD AND TESTING METHOD OF SEMICONDUCTOR CHIP, CAPACITOR AND MANUFACTURING METHOD THEREOF**

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 18, 2003

Sir:

In compliance with 37 CFR 1.56, Applicants call to the attention of the Patent and Trademark Office the references listed on the attached PTO-1449.

A copy of each of the references are enclosed herewith.

In the event there are any fees due in connection with the filing of this paper, please charge Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: PTO-1449; References **(3)**

INFORMATION DISCLOSURE STATEMENT PTO-1449	Atty. Docket No. **030868**	Serial No. **New Application**
	Applicant(s): **Yasuo YAMAGISHI, et al.**	
	Filing Date: **July 18, 2003**	Group Art Unit: **Not Yet Assigned**

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA						
_____	AB						
_____	AC						
_____	AD						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Translation (Yes or No)
_____	AE	EP 0 840 133 A2	05/06/98	EP	
_____	AF	7-111280	04/25/95	Japan	Yes-Abstract/Discussed in the specification
_____	AG	10-132855	05/22/98	Japan	Yes-Abstract/Discussed in the specification
_____	AH				
_____	AI				

OTHER DOCUMENTS

_____	AJ	
_____	AK	

Examiner	Date Considered